body are n-type.

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- 31. The die of claim 29, wherein gate electrode is p-type and the diffusion and the body are n-type, with the diffusion being more heavily doped than the body.
- semiconductor decoupling capacitor further includes a second diffusion coupled to the second conductor to receive the ground voltage and wherein the body receives the ground voltage through the first and second diffusions.
- 33. The die of claim 32, wherein the first and second diffusions are source/drain diffusions.
- 34. (Amended) The die of claim 32, wherein the first and second diffusions are more heavily doped than the body.
- 35. The die of claim 29, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.
- 36. The die of claim 29, wherein gate electrode is p-type and the diffusion and the body are n-type, and wherein the diffusion is a body tap diffusion and the semiconductor decoupling capacitor further includes first and second source/drain diffusions that are p-type.
- 37. The die of claim 36, wherein the first and second source/drain diffusions are coupled to the second conductor to receive the ground voltage.
- 38. The die of claim 36, wherein the body tap diffusion and first and second source/drain diffusions are more heavily doped than the body.
- 39. The die of claim 36, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.
 - 40. A die, comprising:
 - a first conductor carrying a power supply voltage;
 - a second conductor carrying a ground voltage; and
- a semiconductor decoupling capacitor to provide decoupling capacitance between the first and second conductors, the semiconductor decoupling capacitor including:
 - (a) a gate electrode coupled to the second conductor to receive the ground voltage,

- (b) a diffusion coupled to the first conductor to receive the power supply voltage,
- (c) a body to receive the power supply voltage through the diffusion, the semiconductor decoupling capacitor thereby being in depletion mode,
- (d) a substrate, and
- (e) an insulation between the substrate and the body.
- 41. The die of claim 40, wherein gate electrode is n-type and the diffusion and the body are p-type.
- 42. The die of claim 40, wherein gate electrode is n-type and the diffusion and the body are p-type, with the diffusion being more heavily doped than the body.
- 43. The die of claim 40, wherein the diffusion is a first diffusion and the semiconductor decoupling capacitor further includes a second diffusion coupled to the first conductor to receive the power supply voltage and wherein the body receives the power supply voltage through the first and second diffusions.
- 44. The die of claim 43, wherein the first and second diffusions are source/drain diffusions.
- 45. (Amended) The die of claim 43, wherein the first and second diffusions are more heavily doped than the body.
- 46. The die of claim 40, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.
- 47. The die of claim 40, wherein gate electrode is n-type and the diffusion and the body are p-type, and wherein the diffusion is a body tap diffusion and the semiconductor decoupling capacitor further includes first and second source/drain diffusions that are n-type.
- 48. The die of claim 47, wherein the first and second source/drain diffusions are coupled to the second conductor to receive the ground voltage.
- 49. The die of claim 47, wherein the body tap diffusion and first and second source/drain diffusions are more heavily doped than the body.
- 50. The die of claim 47, wherein the semiconductor decoupling capacitor has a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.